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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/734,300	12/15/2003	Yoshiharu Nakajima	SON-1697/DIV	4716

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EXAMINER
DHARIA, PRABODH M

ART UNIT	PAPER NUMBER
2629	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/734,300	NAKAJIMA ET AL.	
	Examiner	Art Unit	
	Prabodh M. Dharia	2629	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *15 December 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-3,10-25,40-45 and 54-58* is/are pending in the application.

4a) Of the above claim(s) *4-9,26-39,46-53 and 59-61* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-3,10-25,40-45 and 54-58* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *15 December 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date *12-15-2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Information Disclosure Statement

2. The information disclosure statement (IDS) submitted on 12-15-2003 w is in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statement is being considered by the examiner.

Drawings

3. Figure 13,1B, 35 and 34 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Specification

4. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed

150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

5. The abstract of the disclosure is objected to because total word count exceeds 150. Correction is required. See MPEP § 608.01(b).

Response to Amendment

6. The amendments filed 12-15-2003 do not introduce any new matter into the disclosure. The added material is supported by the original disclosure.

7. **Status:** Please all the replies and correspondence should be addressed to examiner's new art unit 2629. Receipt is acknowledged of papers submitted on 12-15-2003 under new application, which have been placed of record in the file. Claims 1-3,10-25,40-45 and 54-58 are pending in this action. Claims 4-9, 26-39, 46-53 and 59-61 are cancelled.

Claim Rejections - 35 USC § 102

8. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this

subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

9. Claims 1-3 are rejected under 35 U.S.C. 102(e) as being anticipated by Koyoma et al. (US 6,911,926).

Regarding Claim 1, Koyoma et al. teaches a digital-analog converter circuit for converting (Col. 4, lines 60,61) an n-bit (n is an integer of 2 or more) digital data signal (Col. 4, Lines 62,63) comprising 2n step select units connected across 2n reference voltage lines (Col. 25, Line 5 to Col. 26, Line 3, Col. 5, Lines 15-63, reference voltages are the decoded voltages per logic state of the data bits), each step select unit including n serially connected analog switches polarized to match the a logic state of each data signal n bit (n is an integer of 2 or more), (Col. 5, Lines 15-63, Col. 4, Line 60 to Col. 5, Line 7) and 2n tone select units (Col. 4, Lines 61,62) respectively connected across the outputs of each of the 2n reference voltage lines bit of the n-bit digital data signal (Col. 25, Line 5 to Col. 26, Line 3, Col. 5, Lines 15-63, reference voltages are the decoded voltages per logic state of the data bits, Col. 4, Lines 60-64, Col. 27, Lines 23-38, Col. 38, Line 56 to Col. 39, Line 39, teaches an example of 2n bits being 4 bits).

Regarding Claim 2, Koyoma et al. teaches one conductive type MOS transistor, wherein each of said n analog switches corresponds to the logic of each bit of said data signal comprises a conductive-type MOS transistor (Col. 5, Lines 15-63, Col. 27, Lines 23-38).

Regarding Claim 3, Koyoma et al. teaches the amplitude of said n-bit digital data signal is has a low by an amount amplitude equal to the a reference voltage minimum less a threshold value of the a P-channel MOS transistor in the reference voltage level range and is a high by an amount amplitude equal to the a reference voltage maximum plus a threshold of the an N-channel MOS transistor (Col. 5, Lines 15-63, Col. 27, Lines 23-38, Col. 35, Lines 48-67).

10. Claims 10-25, 40-45, and 54-58 are rejected under 35 U.S.C. 102(e) as being anticipated by Butler (US 6,274,869 B1).

Regarding Claim 10, Butler teaches a level shift circuit having a CMOS latch cell as the basic structure (please see figures 15, 16, Col. 15, Line 59 to Col. 16, Line 5, Col. 16, Lines 42-62) and for converting a low voltage amplitude signal to a high voltage amplitude signal (Col. 16, Lines 20-62) comprising: a CMOS latch cell having two input sections, wherein a first resistor element is inserted respectively between each of the two signal sources and the two input sections of said CMOS latch cell and two signal sources (Col. 15, Line 59 to Col. 16, Line 62).

Regarding Claim 11, Butler teaches first resistor element is a transistor (Col. 24, Lines 63-67, transistor is a resister switches as size of the channel formed between drain and source determines resistive or capacitive transistor switch)

Regarding Claim 12, Butler teaches second resistor elements is element are inserted respectively between a power supply and each of the two input sections of the CMOS latch cell (please see figure 15, Col. 16, Lines 6-64).

Regarding Claim 13, Butler teaches first and said second resistor elements are transistors (Col. 16, Lines 6-64, Col. 24, Lines 63-67 transistor is a resister switches as size of the channel formed between drain and source determines resistive or capacitive transistor switch).

Regarding Claim 14, Butler teaches level shift operation is performed only when a switch is in an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed (Col. 16, Lines 6-64, Col. 24, Lines 63-67).

Regarding Claim 15, Butler teaches level shift circuit has a control circuit to set the switch to the on status only when necessary (Col. 18, Lines 52-67, Lines 21-36).

Regarding Claim 16, Butler teaches said level shift circuit has a reset circuit to determine the an initial status of said CMOS latch cell (Col. 18, Lines 52-67, Lines 21-36, please see figures 15-18).

Regarding Claim 17, Butler teaches a shift register (Col. 18, Line 61-65) comprising a plurality of transfer stages (Col. 18, Lines 57-65) and having a first level shift circuit to supply a

start signal as a level shift to a first stage of the transfer stages (Col. 18, Lines 57-65, Lines 21-36) and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages (Col. 18, Line 52-67) wherein said first and second level shift circuits include a CMOS latch cell having two input sections and a first resistor element inserted between each of the two input sections and two input signal sources (Col. 16, Lines 6-64).

Regarding Claim 18, Butler teaches first resistor element is a transistor (Col. 24, Lines 63-67, transistor is a resister switches as size of the channel formed between drain and source determines resistive or capacitive transistor switch)

Regarding Claim 19, Butler teaches second resistor elements is element are inserted respectively between a power supply and each of the two input sections of the CMOS latch cell (lease see figure 15, Col. 16, Lines 6-64).

Regarding Claim 20, Butler teaches first and said second resistor elements are transistors (Col. 16, Lines 6-64, Col. 24, Lines 63-67 transistor is a resister switches as size of the channel formed between drain and source determines resistive or capacitive transistor switch).

Regarding Claim 21, Butler teaches level shift operation is performed only when said a switch is an on status by utilizing switches having a finite resistance value as said first and said second resistor elements, and at all other times latch operation is performed (Col. 16, Lines 6-64, Col. 24, Lines 63-67).

Regarding Claim 22; Butler teaches shift register has a control circuit to set said switch to the on status only when necessary (Col. 18, Lines 52-67, Lines 21-36).

Regarding Claim 23, Butler teaches shift register has a reset circuit to determine the initial status of said CMOS latch cell (Col. 18, Lines 57-65, Lines 21-36, please see figures 15-18).

Regarding Claim 24, Butler teaches latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28 CMOS semiconductor devices are fabricate on semiconductor substrate like glass or silicon).

Regarding Claim 25, teaches latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28 CMOS semiconductor devices are fabricate on semiconductor substrate like glass or silicon).

Regarding Claim 40, Butler teaches a sampling latch circuit (Col. 17, Lines 32-35) with comprising: a comparator configuration (Col. 17, Lines 33-37) CMOS latch cell (Col. 16, lines 1-5, figures 16-18, Col. 17, Lines 33-37, Col. 15, Line 59 to Col. 16, Line 28) having two input sections; a first switch connected between each of the two input sections (please see figure 16, Col. 15, Lines 59-62) and the two input signal sources; a second switch connected between the a power supply line and the a power supply side of said CMOS latch cell (see figure 16, Col. 15, Lines 59-62, Col. 16, Lines 6-28); and a control means to control complementary switching of

said first switch and said second switch (see figure 16, Col. 15, Lines 59-62, Col. 16, Lines 6-28).

.Regarding Claim 41, Butler teaches first switch and said second switch are transistors (please see figure 16, Col. 15, line 59-Col. 16, Line 28).

Regarding Claim 42, Butler teaches a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuits (Col. 16, Lines 1-5, figures 16-18, Col. 17, Lines 33-47, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 43, Butler teaches also having further comprising: a third switch, synchronized and controlled by said second switch, between the power supply line and the a power supply side of the an output circuit for output of said CMOS latch circuit output signal (Col. 16, Lines 1-5, figures 16-18, Col. 17, Lines 33-37, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 44, Butler teaches second switch is combined with said third switch. (Col. 16, Lines 1-5, figures 16-18, Col. 17, Lines 33-37, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 45, Butler teaches a plurality of said sampling latch circuits are installed and, said second switch is jointly shared by said plurality of sampling latch circuit (Col. 16, Lines 1-5, figures 16-18, Col. 17, Lines 33-47, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 54, Butler teaches latch circuit with including a CMOS latch cell (figure 16, Col. 16, Lines 2-4) having two input sections as a basic structure (Col. 16, lines 6-11), wherein said latch circuit has comprising a first switch and a second switch to respectively select a first and second power supply having different voltages (Col. 15, Lines 59-62, transistors are the switches turning on/off) and installed on at least one of the a positive power side or the a negative power side of said CMOS latch cell (see figure 16, Col. 15, Lines 59-62, Col. 16, Lines 6-28) and, having a control means to control switching of said first and second switches according to the periods of the a latch operation period and an output operation period of said CMOS latch cell (Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 55, Butler teaches first and second switches are transistors (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 56, Butler teaches a plurality of said latch circuits are installed and, said first switch and said second switch are jointly shared by said plurality of sampling latch circuits (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28).

Regarding Claim 57, Butler teaches latch circuit is fabricated by utilizing thin film transistors formed on a glass substrate (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28 CMOS semiconductor devices are fabricate on semiconductor substrate like glass or silicon).

Regarding Claim 58, teaches latch circuit is fabricated by utilizing thin film transistors formed on a silicon substrate (please see figure 16, Col. 15, Line 59 to Col. 16, Line 28 CMOS semiconductor devices are fabricate on semiconductor substrate like glass or silicon).

Double Patenting

11. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., *In re Berg*, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

12. Claims 1-3,10-25, 40-45, and 54-58 are rejected on the ground of nonstatutory double patenting over claims 1-50 of U. S. Patent No. 6,664,943 B1 since the claims, if allowed, would improperly extend the "right to exclude" already granted in the patent.

The subject matter claimed in the instant application is fully disclosed in the patent and is covered by the patent since the patent and the application are claiming common subject matter, as follows: Comparison of Instant application Claims 1-3,10-25, 40-45, and 54-58 to Claims 1-50 of parent applications;

Instant Application Number **10,734,300**	**Parent Applications Number** **09/466/969 and Patent Number** **6,664,943 B1**
1. A digital-analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal comprising 2n step select units connected across 2n reference voltage lines, each step select unit including n serially connected analog switches polarized to match the a logic state of each data signal n bit (n is an integer of 2 or more), and 2n tone select units respectively connected across the outputs of each of the 2n reference voltage lines bit of the n-bit digital data signal.	5. A liquid crystal display device having a first board formed by an effective pixel area comprising a plurality of pixels and a drive circuit containing a digital/analog converter circuit for converting an n-bit (n is an integer of 2 or more) digital data signal, a second board placed at a specified gap facing said first board, and a liquid crystal layer held between said first and said second boards, wherein said digital/analog converter circuit comprises 2.sup.n step select units connected across
10. A level shift circuit having a CMOS latch cell as the basic structure and for converting a low voltage amplitude signal to a high voltage amplitude signal comprising: a CMOS latch cell having two input sections, wherein a first resistor element is inserted respectively	2.sup.n reference voltage lines and pixel section column lines, each step select unit including n serially connected analog switches polarized to match a logic state of each bit of the n-bit digital data signal, a shift register including a plurality of transfer stages to

between each of the two signal sources and the two input sections of said CMOS latch cell and two signal sources. 17.A shift register comprising a plurality of transfer stages and having a first level shift circuit to supply a start signal as a level shift to a first stage of the transfer stages and a second level shift circuit to supply a clock signal as a level shift to each of the transfer stages wherein said first and second level shift circuits include a CMOS latch cell having two input sections and a first resistor element inserted between each of the two input sections and two input signal sources. 40. Latch circuit with including a CMOS latch cell having two input sections as a basic structure, wherein said latch circuit has comprising a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of the a positive power side or the a negative power side of said CMOS latch	output sampling pulses in sequence from each transfer stage by performing a shift operation in response to a start signal; a first latch circuit to synchronize with the sampling pulses output from each transfer stage and sequentially sample and latch the digital data signals; and a second latch circuit to latch the signal sequentially sampled in said first latch circuit with a matching column line at each one horizontal period and supply the latched signal to said digital/analog conversion circuit, wherein said shift register includes a first level shift circuit to supply the start signal to an initial stage of the transfer stages and a second level shift circuit to supply clock signals to each of the transfer stages as a level shift, the first and second level shift circuits including a CMOS latch cell having two input sections and a resistor element inserted between each of the two input sections and two signal sources and wherein said first latch circuit includes a CMOS latch cell having two input sections and

cell and, having a control means to control switching of said first and second switches according to the periods of the a latch operation period and an output operation period of said CMOS latch cell.	a first switch connected between the two input sections and two input signal sources of the said CMOS latch cell, a second switch connected between a power supply line and a power supply side of said CMOS latch cell and, a control means to control complementary
54. Latch circuit with including a CMOS latch cell having two input sections as a basic structure, wherein said latch circuit has comprising a first switch and a second switch to respectively select a first and second power supply having different voltages and installed on at least one of the a positive power side or the a negative power side of said CMOS latch cell and, having a control means to control switching of said first and second switches according to the periods of the a latch operation period and an output operation period of said CMOS latch cell .	switching of said first and said second switches and, wherein said second latch circuit includes a CMOS latch cell having two input sections and a first switch and a second switch installed on at least one of a positive power supply or negative power supply side of the CMOS latch to respectively select a first and a second power supply having different power supply voltages and, a control means to control switching of said first and second switches according to each period of latch operation and output operation of the CMOS latch cell.

Note the comparison above Claims 1,10,17,40 and 54 of instant application to Claim 5 of parent application, the language has been changed to avoid 101 statutory double patenting rejection. However, Claims 1,10,17,40 and 54 of instant application and Claim 5 of parent

application are claiming same limitation. The both applications, the instant as well as parent application are claiming digital/analog converter circuit, a level shift circuit, a shift register containing this level shift circuit, a sampling latch circuit and a latch circuit as well as a liquid crystal display device mounted with these respective circuits; transistor switching devices for the pixels, a level shift circuit in the shift register has a basic structure of CMOS latch cells and is utilized in each level shift of the clock signal at each transfer stage, a sampling latch circuit with a basic structure of CMOS latch cells has a level shift function, stable level shift operation, stable sampling & latch operation in a circuit structure.

Further dependent claims 2,3,11-25, 41-45, and 55-58 of instant application claiming same or similar limitations as dependent and independent claims of parent applications.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Erhart; Richard A et al. (US 5572211 A) Integrated circuit for driving liquid crystal display using multi-level D/A converter.

14. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Prabodh M. Dharia whose telephone number is 571-272-7668. The examiner can normally be reached on M-F 8AM to 5PM.

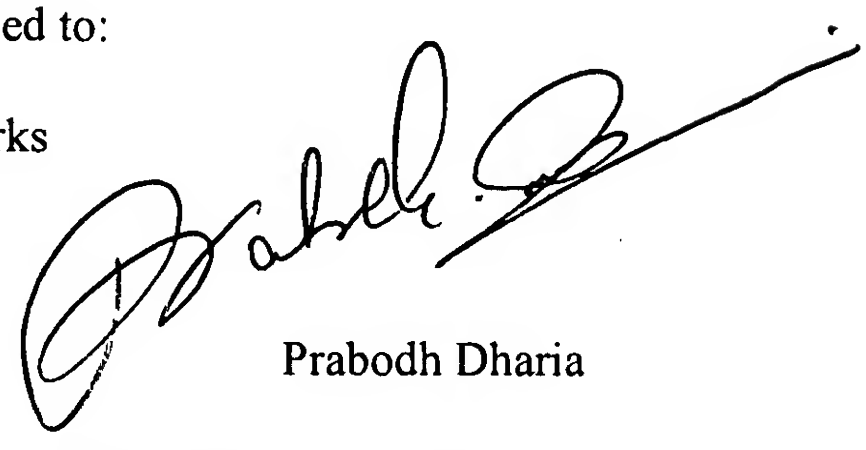
15. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

16. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231



Prabodh Dharia

Partial Signatory Authority

AU2629

May 21, 2007